

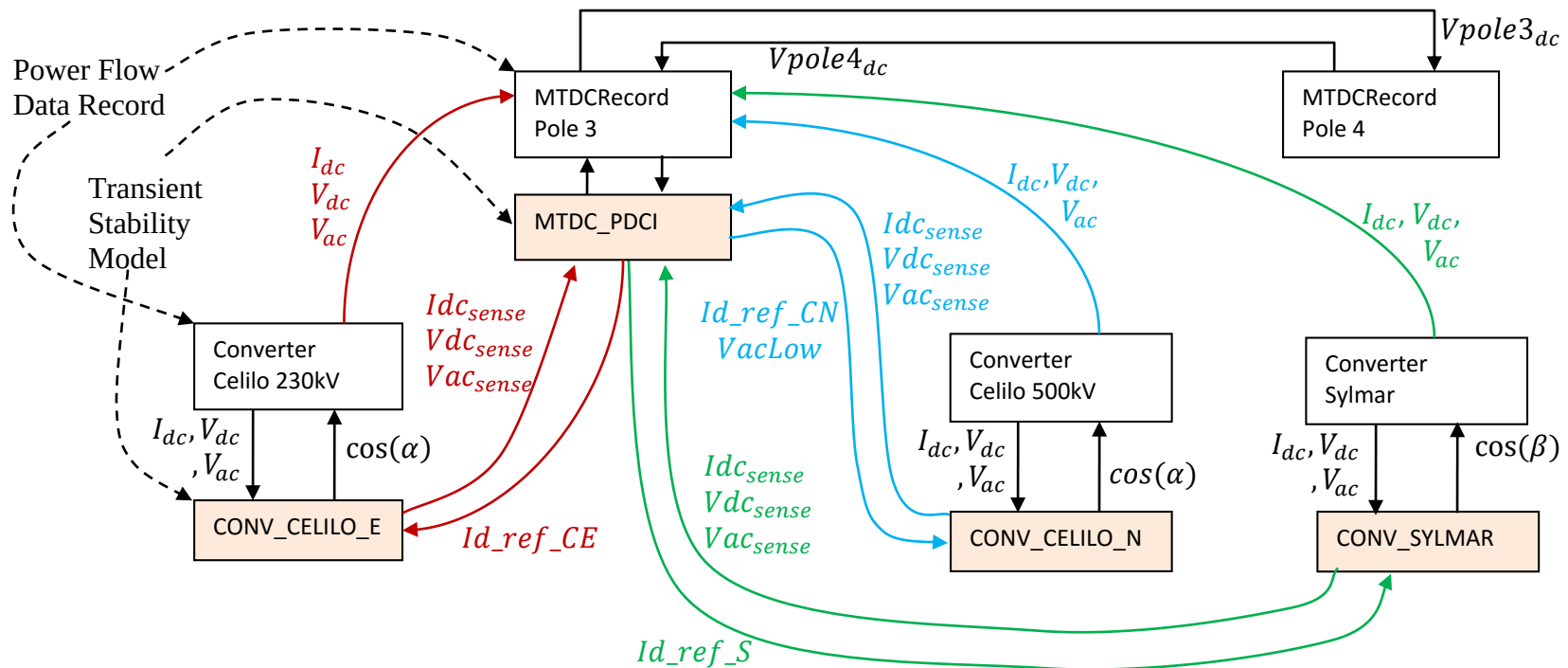
General Overview of Multi-Terminal DC Line Model for the Pacific DC Intertie

Simulator has a multi-terminal DC (MTDC) record which represents the grouping of the dc converters, dc buses and dc lines for a single pole of a MTDC transmission line. The Pacific DC Intertie (PDCI) is represented by two of these records: one for each pole of the PDCI. For the PDCI, each MTDC record contains three DC converters with two at Celilo (North end) and one at Sylmar (South end). In Simulator these DC converters are also represented by unique objects.

The transient stability model of the PDCI works by assigning a dynamic model to each of the two MTDC records, and also assigning a dynamic model to each of the DC converter objects. To model this, there are 4 dynamic models

MTDC_PDCI	Assigned to the MTDC record.
CONV_CELILO_E	Assigned to the Celilo DC converter at the 230 kV bus at Celilo (North). Note: "E" stands for "existing"
CONV_CELILO_N	Assigned to the Celilo DC converter at the 500 kV bus at Celilo (North). Note: "N" stands for "new"
CONV_SYLMAR	Assigned to the DC converter at Sylmar (South)

The flow of signals is depicted in the following image.



The function of the converts is generally described as follows.

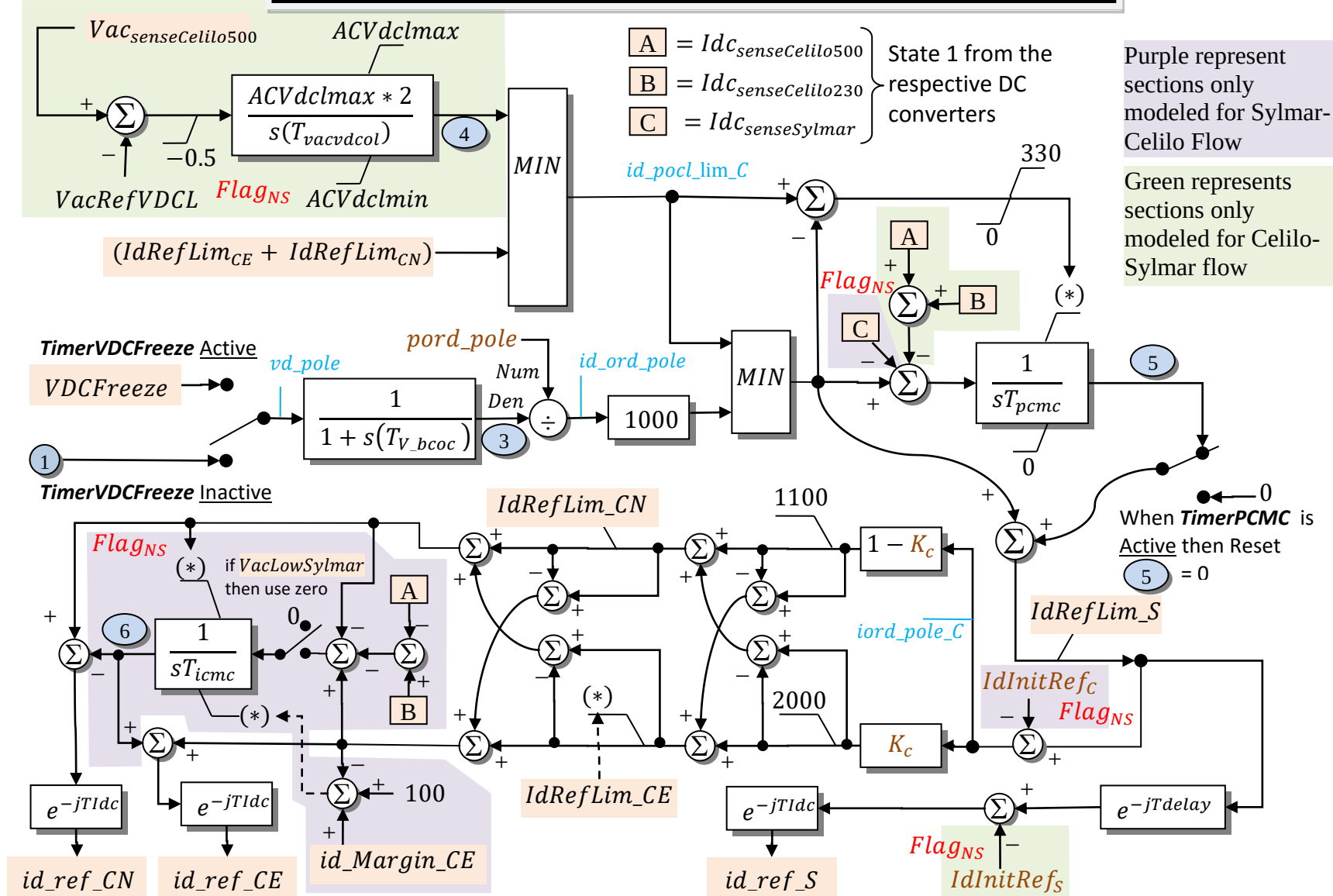
MTDC_PDCI	Assigned to the MTDC record. Model will coordinate the allocation of current order reference signals sent to the three DC converters that it manages. Model may also pass on various flags such a <i>VacLow</i> . Model receives signals of sensed AC and DC voltage and DC current from the converters also. The two MTDC_PDCI models will act independently of one another, except that each record passes a measurement of the DC voltage at the rectifier end of each pole to the other pole.
CONV_CELILO_E	Assigned to the "existing" Celilo DC converter at the 230 kV bus at Celilo (North). Converter initializes its Isched and Psched values to those from the initial network boundary equation solution. Model will take as an input one signals from MTDC_PDCI: the current order reference signal (<i>Id_ref_CE</i>).
CONV_CELILO_N	Assigned to the "new" Celilo DC converter at the 500 kV bus at Celilo (North). Converter initializes its Isched and Psched values to those from the initial network boundary equation solution. Model will take as an input two signals from MTDC_PDCI: the current order reference signal (<i>Id_ref_CN</i>) and the flag <i>VacLow</i> .
CONV_SYLMAR	Assigned to the DC converter at Sylmar (South). Converter initializes its Isched and Psched values to those from the initial network boundary equation solution. Model will take as an input one signalsfrom MTDC_PDCI: the current order reference signal (<i>Id_ref_S</i>).

In addition the implementation of these four models will be automatically modify based on the initial flow in the initial system flow direction (depending whether the flow is from Celilo to Sylmar or Sylmar to Celilo). These modifications reflect the differences in how each converter behaves when acting as a rectifier or inverter. In the following block diagrams portions of the model which are only used for a flow from Celilo to Sylmar (North to South) are highlighted in green, while portion only used for a flow from Sylmar to Celilo (North to South) are highlighted in purple. Differences also have a red notation of *Flag_{NS}* added to denote highlighting. Values which are passed between models are highlighted in orange. Outputs of the control angle for DC converters are highlighted in pink.

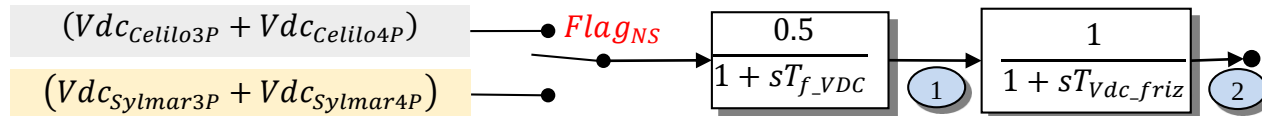
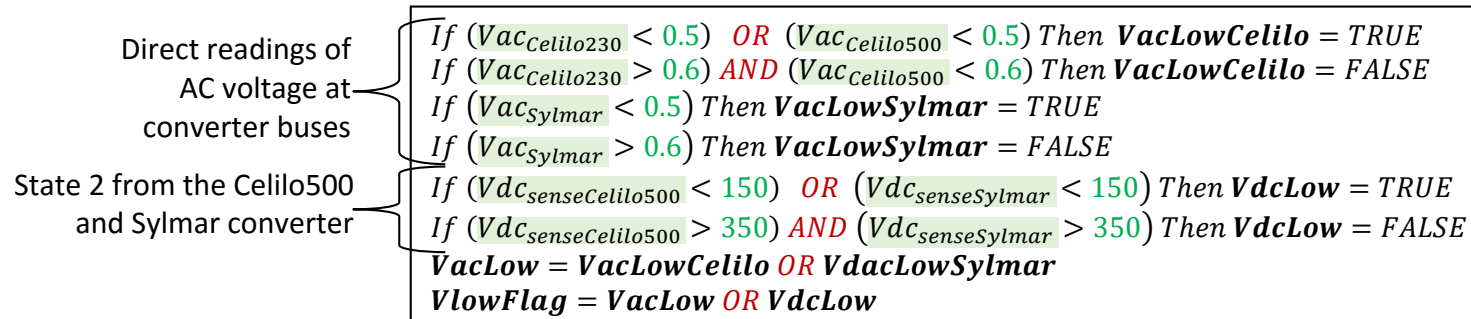
State 3 from the
Celilo 500 converter

MTDC_PDCI

Current Order Allocation Calculations for Celilo and Sylmar



MTDC_PDCI (North to South Implementation) Measurements and Low Voltage Detection Logic



DC Voltage Measurement Freeze

If **VLowFlag** = TRUE then activate a timer **TimerVDCFreeze** and set timer to **Tdel_{friz}**. Continue to set this timer up to **Tdel_{friz}** as long as **VLowFlag** is TRUE. If **VLowFlag** become FALSE then start having the timer count down to zero. Once the **TimerVDCFreeze** reaches zero then make it inactive.

Whenever **TimerVDCFreeze** is inactive then

Set **VDCFreeze** = **2**

and pass **1** as the DC voltage to Current Order Allocation Calculation

Whenever **TimerVDCFreeze** is active then

Pass the variable **VDCFreeze** as the DC voltage to the Current Order Calculation

Pole Current Margin Compensator

If **VLowFlag** = TRUE then activate a timer **TimerPCMC** and set timer to **Tpcmc_rst**. Continue to set this timer up to **Tpcmc_rst** as long as **VLowFlag** is TRUE. If **VLowFlag** become FALSE then start having the timer count down to zero. Once the **TimerPCMC** reaches zero then make it inactive.

MTDC_PDCI Parameters are all hard-coded based on whether the initial flow direction of the PDCI. The parameters and the initialization are different for Celilo to Sylmar (North to South) or Sylmar to Celilo (South to North) flow. The following table shows the differences

Parameter	Celilo-Sylmar (North to South)	Sylmar - Celilo (South to North)
T_{fpcmc_rst}	0.1	
T_{VDC_friz}	0.53	
$Tdel_{friz}$	0.44	
$VacRefVDCL$	228/230	n/a
$ACVdclmax$	3100	n/a
$ACVdclmin$	2400	n/a
$T_{vacavdcol}$	0.5	n/a
$IdRefLim_{CE}$	Get from CONV_CELILO_E model	
$IdRefLim_{CN}$	Get from CONV_CELILO_N model	
$IdRefLim_S$	Get from CONV_SYLMAR model	
T_{v_bcoc}	0.05	
T_{pcmc}	0.5120	
T_{icmc}	n/a	0.2500
Id_margin_CE	Get from CONV_CELILO_E model	
$TIdc$	0.5 cycles	
$Tdelay$	2 cycles	

Initialization Reference Values	Celilo-Sylmar (North to South)	Sylmar - Celilo (South to North)
$pord_pole$	Initialize to Sum of Psched at two Celilo Converters	Initialize to Psched at the Sylmar Converter
K_c	Initialize based on the following equation $K_c = \frac{id_ref_CE}{id_ref_CE + id_ref_CN}$	
$VacLowSylmar$	FALSE	
$VacLowCelilo$	FALSE	
$VdcLow$	FALSE	
$VLowFlag$	FALSE	
$IdInitRef_C$	n/a	Initialize equal to State 14 to handle difference between id_ord_pole and id_ref_S
$IdInitRef_S$	Initialize equal to State 14 to handle difference between id_ord_pole and id_ref_CN + id_ref_CE	n/a